

1994 Index

IEEE Transactions on Semiconductor Manufacturing

Vol. 7

This index covers all technical items — papers, correspondence, reviews, etc. — that appeared in this periodical during 1994, and items from previous years that were commented upon or corrected in 1994.

The Author Index contains the primary entry for each item, listed under the first author's name, and cross-references from all coauthors. The Subject Index contains several entries for each item under appropriate subject headings, and subject cross-references.

It is always necessary to refer to the primary entry in the Author Index for the exact title, coauthors, and comments/corrections.

AUTHOR INDEX

A

- Ajioka, T., *see* Mizokami, Y., *T-SEM Nov 94* 447-453
 Allen, R.A., *see* Cresswell, M.W., *T-SEM Aug 94* 266-271
 Apte, P.P., *see* Saraswat, K.C., *T-SEM May 94* 159-175
 Au, R., *see* Shimada, H., *T-SEM Aug 94* 389-393

B

- Banerjee, H., *see* Khotanzad, A., *T-SEM Nov 94* 413-422
 Banerjee, S., *see* Maung, S., *T-SEM May 94* 184-192
 Barna, G.G., *see* Mozumder, P.K., *T-SEM Feb 94* 1-11
 Barna, G.G., L.M. Loewenstein, R. Robbins, S. O'Brien, A. Lane, D.D. White, Jr., M. Hanratty, J. Hosch, G.B. Shinn, K. Taylor, and K. Brankner. MMST manufacturing technology-hardware, sensors, and processes; *T-SEM May 94* 149-158
 Beaver, R., A. Coleman, D. Draheim, and A. Hoffman. Architecture and overview of MMST machine control [semiconductor manufacturing facilities]; *T-SEM May 94* 127-133
 Blaes, B.R., and M.G. Buehler. SEU/SRAM as a process monitor; *T-SEM Aug 94* 319-324
 Boning, D.S., and P.K. Mozumder. DOE/Opt: a system for design of experiments, response surface modeling, and optimization using process and device simulation; *T-SEM May 94* 233-244
 Booth, L., *see* Saraswat, K.C., *T-SEM May 94* 159-175
 Boskin, E.D., C.J. Spanos, and G.J. Korsh. A method for modeling the manufacturability of IC designs; *T-SEM Aug 94* 298-305
 Brankner, K., *see* Barna, G.G., *T-SEM May 94* 149-158
 Buehler, M.G., *see* Blaes, B.R., *T-SEM Aug 94* 319-324
 Buller, J.F., *see* Farahani, M.M., *T-SEM Feb 94* 79-86
 Butler, S.W., *see* Sullivan, M., *T-SEM May 94* 134-148
 Butler, S.W., *see* Maung, S., *T-SEM May 94* 184-192
 Butler, S.W., and J.A. Stefani. Supervisory run-to-run control of polysilicon gate etch using in situ ellipsometry; *T-SEM May 94* 193-201
 Byung Jin Cho, P. Vandenabeele, and K. Maex. Development of a hexagonal-shaped rapid thermal processor using a vertical tube; *T-SEM Aug 94* 345-353
 Byungwhan Kim, and G.S. May. An optimal neural network process model for plasma etching; *T-SEM Feb 94* 12-21

C

- Campbell, S.A., *see* Knutson, K.L., *T-SEM Feb 94* 68-72
 Cavin, R.K., III, *see* Perkinson, T.L., *T-SEM Aug 94* 369-373
 Cerrina, F., *see* Pan, S., *T-SEM Aug 94* 325-332
 Chatterjee, P.K., and P.K. Mozumder. Editorial: Special issue on microelectronics manufacturing science and technology [intro.]; *T-SEM May 94* 106
 Cho, Y.M., A. Paulraj, T. Kailath, and Guanghan Xu. A contribution to optimal lamp design in rapid thermal processing; *T-SEM Feb 94* 34-41
 Coleman, A., *see* Beaver, R., *T-SEM May 94* 127-133
 Collins, D.J., A.J. Strojwas, and D.D. White, Jr. A CFD model for the PECVD of silicon nitride; *T-SEM May 94* 176-183
 Collins, D.J., *see* Mozumder, P.K., *T-SEM Aug 94* 400-411
 Compton, S., *see* Zhen-Hong Zhou, *T-SEM Feb 94* 87-91
 Craigin, B., *see* Parks, H.G., *T-SEM Aug 94* 249-258

- Cresswell, M.W., R.A. Allen, L.W. Linholm, C.H. Ellenwood, W.B. Penzes, and E.C. Teague. New test structure for nanometer-level overlay and feature-placement metrology; *T-SEM Aug 94* 266-271

D

- Dankoski, P.C.P., *see* Saraswat, K.C., *T-SEM May 94* 159-175
 Degertekin, F.L., *see* Saraswat, K.C., *T-SEM May 94* 159-175
 de Gyvez, J.P. Mound defect modeling in yield forecasts; *T-SEM Nov 94* 430-439
 Di Fabrizio, E., *see* Pan, S., *T-SEM Aug 94* 325-332
 Dimitrijevic, S., *see* Sitte, R., *T-SEM Feb 94* 92-96
 Donnellan, B., *see* Power, J.A., *T-SEM Aug 94* 306-318
 Draheim, D., *see* Beaver, R., *T-SEM May 94* 127-133
 Draheim, D., *see* Maung, S., *T-SEM May 94* 184-192
 Dunn, F., *see* Knutson, K.L., *T-SEM Feb 94* 68-72

E

- Edgar, T.F., *see* Huang, Y.L., *T-SEM Aug 94* 333-344
 Ellenwood, C.H., *see* Cresswell, M.W., *T-SEM Aug 94* 266-271
 Eriguchi, K., *see* Uraoka, Y., *T-SEM Aug 94* 293-297

F

- Fallon, M., A.J. Walton, J.T.M. Stevenson, and A.W.S. Ross. Design considerations for a Gaudi test structure which can be used to determine the optimum focus; *T-SEM Aug 94* 272-278
 Farahani, M.M., J.F. Buller, B.T. Moore, and S. Garg. Conventional contact interconnect technology as an alternative to contact plug (W) technology for 0.85 μm CMOS EPROM IC devices; *T-SEM Feb 94* 79-86
 Fargher, H.E., M.A. Kilgore, P.J. Kline, and R.A. Smith. A planner and scheduler for semiconductor manufacturing; *T-SEM May 94* 117-126
 Franklin, G.F., *see* Saraswat, K.C., *T-SEM May 94* 159-175

G

- Garg, S., *see* Farahani, M.M., *T-SEM Feb 94* 79-86
 Gaston, G.J., and A.J. Walton. The integration of simulation and response surface methodology for the optimization of IC processes; *T-SEM Feb 94* 22-33
 Groover, R., W.K. Shu, and S.S. Lee. Wire bond loop profile development for fine pitch-long wire assembly; *T-SEM Aug 94* 393-399
 Guanghan Xu, *see* Cho, Y.M., *T-SEM Feb 94* 34-41
 Guzzo, E.E., and J.S. Preston. Laser ablation as a processing technique for metallic and polymer layered structures; *T-SEM Feb 94* 73-78
 Gyugyi, P.J., *see* Saraswat, K.C., *T-SEM May 94* 159-175
 Gyurcsik, R.S., *see* Perkinson, T.L., *T-SEM Aug 94* 369-373

H

- Hanratty, M., *see* Barna, G.G., *T-SEM May 94* 149-158
 Harrison, H.B., *see* Sitte, R., *T-SEM Feb 94* 92-96
 Hasnat, K., S. Murtaza, and A.F. Tasch, Jr. A manufacturing sensitivity analysis of 0.35 μm LDD MOSFET's; *T-SEM Feb 94* 53-59
 Hebley, J., *see* McGehee, J., *T-SEM May 94* 107-116
 Henck, S., *see* Maung, S., *T-SEM May 94* 184-192
 Hess, C., and A.P. Stroele. Modeling of real defect outlines and parameter extraction using a checkerboard test structure to localize defects; *T-SEM Aug 94* 284-292
 Himmelblau, D.M., *see* Huang, Y.L., *T-SEM Aug 94* 333-344
 Hiraiwa, A., and T. Itoga. Scaling law in ULSI contamination control; *T-SEM Feb 94* 60-67
 Hirasawa, S., T. Watanabe, T. Takagaki, and T. Uchino. Temperature distribution in semiconductor wafers heated in a hot-wall-type rapid diffusion furnace; *T-SEM Nov 94* 423-429
 Hirsch, J., *see* Sullivan, M., *T-SEM May 94* 134-148
 Hoffman, A., *see* Beaver, R., *T-SEM May 94* 127-133
 Hosch, J., *see* Barna, G.G., *T-SEM May 94* 149-158

Huang, Y.L., T.F. Edgar, D.M. Himmelblau, and I. Trachtenberg. Constructing a reliable neural network model for a plasma etching process using limited experimental data; *T-SEM Aug 94* 333-344

I

Itoga, T., see Hiraiwa, A., *T-SEM Feb 94* 60-67
Iwata, H., see Ohzone, T., *T-SEM Aug 94* 259-265

J

Jones, R., see Parks, H.G., *T-SEM Aug 94* 249-258

K

Kailath, T., see Cho, Y.M., *T-SEM Feb 94* 34-41
Kailath, T., see Schaper, C., *T-SEM May 94* 202-219
Khare, J.B., W. Maly, and M.E. Thomas. Extraction of defect size distributions in an IC layer using test structure data; *T-SEM Aug 94* 354-368
Khotanzad, A., H. Banerjee, and M.D. Srinath. A vision system for inspection of ball bonds and 2-D profile of bonding wires in integrated circuits; *T-SEM Nov 94* 413-422
Khuri-Yakub, B.T., see Saraswat, K.C., *T-SEM May 94* 159-175
Kiether, W.J., see Sorrell, F.Y., *T-SEM Nov 94* 454-459
Kilgore, M.A., see Fargher, H.E., *T-SEM May 94* 117-126
Kline, P.J., see Fargher, H.E., *T-SEM May 94* 117-126
Knutson, K.L., S.A. Campbell, and F. Dunn. Modeling of three-dimensional effects on temperature uniformity in rapid thermal processing of eight inch wafers; *T-SEM Feb 94* 68-72
Korsh, G.J., see Boskin, E.D., *T-SEM Aug 94* 298-305
Kowng, V., see Pan, Y., *T-SEM Nov 94* 460-462
Kumar, P.R., see Lu, S.C.H., *T-SEM Aug 94* 374-388
Kure, T., see Tamaki, Y., *T-SEM Aug 94* 279-283

L

Lane, A., see Barna, G.G., *T-SEM May 94* 149-158
Lane, W.A., see Power, J.A., *T-SEM Aug 94* 306-318
Lee, S.S., see Groover, R., *T-SEM Aug 94* 393-399
Lee, Y.J., see Saraswat, K.C., *T-SEM May 94* 159-175
Leonard, Q., see Pan, S., *T-SEM Aug 94* 325-332
Liehr, M., see Rubloff, G.W., *T-SEM Feb 94* 96-100
Linholt, L.W. Guest editorial [intro. to the special issue on ICMTS '93]; *T-SEM Aug 94* 246
Linholt, L.W., see Cresswell, M.W., *T-SEM Aug 94* 266-271
Loewenstein, L.M., see Barna, G.G., *T-SEM May 94* 149-158
Lu, S.C.H., D. Ramaswamy, and P.R. Kumar. Efficient scheduling policies to reduce mean and variance of cycle-time in semiconductor manufacturing plants; *T-SEM Aug 94* 374-388

M

Maex, K., see Byung Jin Cho, *T-SEM Aug 94* 345-353
Mahaffey, J., see McGehee, J., *T-SEM May 94* 107-116
Maly, W., see Khare, J.B., *T-SEM Aug 94* 354-368
Mathewson, A., see Power, J.A., *T-SEM Aug 94* 306-318
Maung, S., S. Banerjee, D. Draheim, S. Henck, and S.W. Butler. Integration of in situ spectral ellipsometry with MMST machine control; *T-SEM May 94* 184-192
May, G.S., see Byungwhan Kim, *T-SEM Feb 94* 12-21
McGehee, J., J. Hebley, and J. Mahaffey. The MMST computer-integrated manufacturing system framework; *T-SEM May 94* 107-116
McLarty, P.K., see Perkinson, T.L., *T-SEM Aug 94* 369-373
Mishima, H., see Ohmi, T., *T-SEM Nov 94* 440-446
Miyawaki, M., see Shimada, H., *T-SEM Aug 94* 389-393
Mizokami, Y., T. Ajioka, and N. Terada. Chemical analysis of metallic contamination on a wafer after wet cleaning; *T-SEM Nov 94* 447-453
Moore, B.T., see Farahani, M.M., *T-SEM Feb 94* 79-86
Moslehi, M., see Schaper, C., *T-SEM May 94* 202-219
Moslehi, M.M., see Saraswat, K.C., *T-SEM May 94* 159-175
Mozumder, P.K., and G.G. Barna. Statistical feedback control of a plasma etch process; *T-SEM Feb 94* 1-11
Mozumder, P.K., see Chatterjee, P.K., *T-SEM May 94* 106
Mozumder, P.K., see Boning, D.S., *T-SEM May 94* 233-244
Mozumder, P.K., S. Saxena, and D.J. Collins. A monitor wafer based controller for semiconductor processes; *T-SEM Aug 94* 400-411

Murtaza, S., see Hasnat, K., *T-SEM Feb 94* 53-59

N

Nakamura, T., see Tamaki, Y., *T-SEM Aug 94* 279-283
Ng, K.K., see Pan, Y., *T-SEM Nov 94* 460-462

O

O'Brien, S., see Barna, G.G., *T-SEM May 94* 149-158
Offenberg, M., see Rubloff, G.W., *T-SEM Feb 94* 96-100
Ohmi, T., see Shimada, H., *T-SEM Aug 94* 389-393
Ohmi, T., S. Sudoh, and H. Mishima. Static charge removal with IPA solution; *T-SEM Nov 94* 440-446
Ohzone, T., and H. Iwata. Channel-width measurements of LOCOS- and trench-isolated MOSFET's by photoemission; *T-SEM Aug 94* 259-265

P

Pan, S., M.T. Reilly, E. Di Fabrizio, Q. Leonard, J.W. Taylor, and F. Cerrina. An optimization design method for chemically amplified resist process control; *T-SEM Aug 94* 325-332
Pan, Y., V. Kowng, and K.K. Ng. A new method for detecting the polysilicon gate reentrant of the submicron LDD MOSFET's; *T-SEM Nov 94* 460-462
Parks, H.G., R.D. Schrimpf, B. Craigin, R. Jones, and P. Resnick. Quantifying the impact of homogeneous metal contamination using test structure metrology and device modeling; *T-SEM Aug 94* 249-258
Paulraj, A., see Cho, Y.M., *T-SEM Feb 94* 34-41
Pei, J., see Saraswat, K.C., *T-SEM May 94* 159-175
Penzes, W.B., see Cresswell, M.W., *T-SEM Aug 94* 266-271
Perkinson, T.L., P.K. McLarty, R.S. Gyurcsik, and R.K. Cavin, III. Single-wafer cluster tool performance: an analysis of throughput; *T-SEM Aug 94* 369-373
Power, J.A., B. Donnellan, A. Mathewson, and W.A. Lane. Relating statistical MOSFET model parameter variabilities to IC manufacturing process fluctuations enabling realistic worst case design; *T-SEM Aug 94* 306-318
Preston, J.S., see Guzzo, E.E., *T-SEM Feb 94* 73-78

R

Ramamurthi, R.K. Self-learning fuzzy logic system for in situ, in-process diagnostics of mass flow controller (MFC); *T-SEM Feb 94* 42-52
Ramaswamy, D., see Lu, S.C.H., *T-SEM Aug 94* 374-388
Reif, R., see Zhen-Hong Zhou, *T-SEM Feb 94* 87-91
Reilly, M.T., see Pan, S., *T-SEM Aug 94* 325-332
Resnick, P., see Parks, H.G., *T-SEM Aug 94* 249-258
Robbins, R., see Barna, G.G., *T-SEM May 94* 149-158
Ross, A.W.S., see Fallon, M., *T-SEM Aug 94* 272-278
Rubloff, G.W., M. Offenberg, and M. Liehr. Integrated processing of MOS gate dielectric structures; *T-SEM Feb 94* 96-100

S

Saraswat, K., see Schaper, C., *T-SEM May 94* 202-219
Saraswat, K.C., P.P. Apte, L. Booth, Yunzhong Chen, P.C.P. Dankoski, F.L. Degertekin, G.F. Franklin, B.T. Khuri-Yakub, M.M. Moslehi, C. Schaper, P.J. Gyugyi, Y.J. Lee, J. Pei, and S.C. Wood. Rapid thermal multiprocessing for a programmable factory for adaptable manufacturing of ICs; *T-SEM May 94* 159-175
Saxena, S., and A. Unruh. Diagnosis of semiconductor manufacturing equipment and processes; *T-SEM May 94* 220-232
Saxena, S., see Mozumder, P.K., *T-SEM Aug 94* 400-411
Schaper, C., see Saraswat, K.C., *T-SEM May 94* 159-175
Schaper, C., M. Moslehi, K. Saraswat, and T. Kailath. Control of MMST RTP: repeatability, uniformity, and integration for flexible manufacturing [ICs]; *T-SEM May 94* 202-219
Schrimpf, R.D., see Parks, H.G., *T-SEM Aug 94* 249-258
Shiba, T., see Tamaki, Y., *T-SEM Aug 94* 279-283
Shimada, H., S. Shimomura, R. Au, M. Miyawaki, and T. Ohmi. Enhancement of resolution and linearity control of contact-hole resist patterns with surface-active developer; *T-SEM Aug 94* 389-393
Shimomura, S., see Shimada, H., *T-SEM Aug 94* 389-393
Shinn, G.B., see Barna, G.G., *T-SEM May 94* 149-158
Shu, W.K., see Groover, R., *T-SEM Aug 94* 393-399

- Sitte, R.**, S. Dimitrijević, and H.B. Harrison. The effect of dynamic design processing for yield enhancement in the fabrication of deep sub-micron MOSFET's; *T-SEM Feb 94* 92-96
- Smith, R.A.**, see Fargher, H.E., *T-SEM May 94* 117-126
- Sorrell, F.Y.**, S. Yu, and W.J. Kiether. Applied RTP optical modeling: An argument for model-based control; *T-SEM Nov 94* 454-459
- Spanos, C.J.**, see Boskin, E.D., *T-SEM Aug 94* 298-305
- Srinath, M.D.**, see Khotanzad, A., *T-SEM Nov 94* 413-422
- Stefani, J.A.**, see Butler, S.W., *T-SEM May 94* 193-201
- Stevenson, J.T.M.**, see Fallon, M., *T-SEM Aug 94* 272-278
- Stroele, A.P.**, see Hess, C., *T-SEM Aug 94* 284-292
- Strojwas, A.J.**, see Collins, D.J., *T-SEM May 94* 176-183
- Sudoh, S.**, see Ohmi, T., *T-SEM Nov 94* 440-446
- Sullivan, M.**, S.W. Butler, J. Hirsch, and C.J. Wang. A control-to-target architecture for process control; *T-SEM May 94* 134-148

T

- Takagaki, T.**, see Hirasawa, S., *T-SEM Nov 94* 423-429
- Tamaki, T.**, see Uraoka, Y., *T-SEM Aug 94* 293-297
- Tamaki, Y.**, T. Shiba, T. Kure, and T. Nakamura. A new test structure for the evaluation of graft-base lateral diffusion depth in high-performance bipolar transistors; *T-SEM Aug 94* 279-283
- Tasch, A.F., Jr.**, see Hasnat, K., *T-SEM Feb 94* 53-59
- Taylor, J.W.**, see Pan, S., *T-SEM Aug 94* 325-332
- Taylor, K.**, see Barna, G.G., *T-SEM May 94* 149-158
- Teague, E.C.**, see Cresswell, M.W., *T-SEM Aug 94* 266-271
- Terada, N.**, see Mizokami, Y., *T-SEM Nov 94* 447-453
- Thomas, M.E.**, see Khare, J.B., *T-SEM Aug 94* 354-368
- Trachtenberg, I.**, see Huang, Y.L., *T-SEM Aug 94* 333-344
- Tsuji, K.**, see Uraoka, Y., *T-SEM Aug 94* 293-297

U

- Uchino, T.**, see Hirasawa, S., *T-SEM Nov 94* 423-429
- Unruh, A.**, see Saxena, S., *T-SEM May 94* 220-232
- Uraoka, Y.**, K. Eriguchi, T. Tamaki, and K. Tsuji. Evaluation technique of gate oxide damage; *T-SEM Aug 94* 293-297

V

- Vandenabeele, P.**, see Byung Jin Cho, *T-SEM Aug 94* 345-353

W

- Walton, A.J.**, see Gaston, G.J., *T-SEM Feb 94* 22-33
- Walton, A.J.**, see Fallon, M., *T-SEM Aug 94* 272-278
- Wang, C.J.**, see Sullivan, M., *T-SEM May 94* 134-148
- Watanabe, T.**, see Hirasawa, S., *T-SEM Nov 94* 423-429
- White, D.D., Jr.**, see Barna, G.G., *T-SEM May 94* 149-158
- White, D.D., Jr.**, see Collins, D.J., *T-SEM May 94* 176-183
- Wood, S.C.**, see Saraswat, K.C., *T-SEM May 94* 159-175

Y

- Yang, I.**, see Zhen-Hong Zhou, *T-SEM Feb 94* 87-91
- Yu, S.**, see Sorrell, F.Y., *T-SEM Nov 94* 454-459
- Yunzhong Chen**, see Saraswat, K.C., *T-SEM May 94* 159-175

Z

- Zhen-Hong Zhou**, S. Compton, I. Yang, and R. Reif. In situ semiconductor materials characterization by emission Fourier transform infrared spectroscopy; *T-SEM Feb 94* 87-91

SUBJECT INDEX

A

Ablation

- microelectronic proc. tech., polymer/metallic layered struct. *Guzzo, E.E.*, +, *T-SEM Feb 94* 73-78

Adaptive control

- PECVD monitor wafer based controller for semicond. procs. *Mozumder, P.K.*, +, *T-SEM Aug 94* 400-411

Air insulation; cf. Electrostatic discharges

Automatic optical inspection

- IC ball bond inspection/2-D bonding wire profiling, vision system. *Khotanzad, A.*, +, *T-SEM Nov 94* 413-422
- real defect outlines and param. extraction, IC checkerboard test struct. *Hess, C.*, +, *T-SEM Aug 94* 284-292

Automated optical inspection; cf. Inspection, visual

Awards

- IEEE Trans. on Semicond. Manufacturing Best Paper Award given to Y.M. Cho and T. Kailath. *T-SEM Aug 94* 245

B

Bipolar transistors

- graft-base lateral diffusion depth in high-perform. bipolar transistors. *Tamaki, Y.*, +, *T-SEM Aug 94* 279-283

Bonding; cf. Integrated circuit bonding

Breakdown; cf. Semiconductor device breakdown

C

CAD (computer-aided design); cf. Design automation

Calibration

- mass flow controllers in semicond. mfg., fuzzy logic syst. *Ramamurthi, R.K.*, *T-SEM Feb 94* 42-52

Circuit radiation effects; cf. Integrated circuit radiation effects

Circuit reliability; cf. Integrated circuit reliability

Circuit simulation

- CMOS stat. MOSFET model, IC mfg. proc. fluc., worst case design. *Power, J.A.*, +, *T-SEM Aug 94* 306-318
- IC proc. optim., simul./response surface methodology integrat. *Gaston, G.J.*, +, *T-SEM Feb 94* 22-33

CMOSFETs

- CMOSFETs, integrated proc. of MOS gate dielec. structs. *Rubloff, G.W.*, +, *T-SEM Feb 94* 96-100

CMOS integrated circuits

- manufacturability enhancements model, measurable proc. params. *Boskin, E.D.*, +, *T-SEM Aug 94* 298-305
- stat. MOSFET model, IC mfg. proc. fluc., worst case design. *Power, J.A.*, +, *T-SEM Aug 94* 306-318
- submicron LDD p-MOSFETs, poly-Si gate reentrant detect. *Pan, Y.*, +, *T-SEM Nov 94* 460-462
- ULSI, homog. metal contamination, test struct. metrology. *Parks, H.G.*, +, *T-SEM Aug 94* 249-258

CMOS integrated circuits, memory

- EPROM IC devices, 0.85- μ m, conventional contact interconnect technol. *Farahani, M.M.*, +, *T-SEM Feb 94* 79-86
- SEU/SRAM, CMOS proc. monitor. *Blaes, B.R.*, +, *T-SEM Aug 94* 319-324

Computer-aided design; cf. Design automation

Computer applications; cf. Distributed computing; Neural network applications

Computer integrated manufacturing

- MMST CIM syst. framework for semicond. wafer fab. *McGehee, J.*, +, *T-SEM May 94* 107-116
- MMST IC mfg. equip. control, situ spectral ellipsometry. *Maung, S.*, +, *T-SEM May 94* 184-192
- MMST machine control archit. for semicond. mfg. facilities. *Beaver, R.*, +, *T-SEM May 94* 127-133
- MMST mfg. technol., hardware, sens., and procs. *Barna, G.G.*, +, *T-SEM May 94* 149-158
- rapid thermal multiprocessing for prog. factory in IC mfg. *Saraswat, K.C.*, +, *T-SEM May 94* 159-175
- run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M.*, +, *T-SEM May 94* 134-148
- semicond. mfg., planner and scheduler. *Fargher, H.E.*, +, *T-SEM May 94* 117-126

Computer vision; cf. Machine vision

Conducting films

- laser ablation proc. tech. for metallic/polymer layered struct. *Guzzo, E.E.*, +, *T-SEM Feb 94* 73-78

Contact resistance

- CMOS EPROM IC devices, 0.85- μ m, conventional contact interconnect technol. *Farahani, M.M.*, +, *T-SEM Feb 94* 79-86

Contamination; cf. Integrated circuit fabrication; Integrated circuit manufacture
Control systems; cf. Adaptive control; Fluid flow control; Fuzzy control; Intelligent control; Learning control systems; Multivariable systems; Predictive control; Process control; Temperature control

D

Data acquisition

run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. Sullivan, M., +, *T-SEM May 94* 134-148

Data processing; cf. Manufacturing data processing

Design automation

CMOS stat. MOSFET model, IC mfg. proc. fluc., worst case design. Power, J.A., +, *T-SEM Aug 94* 306-318

DOE/Opt syst. for semicond. mfg. proc./device modelling/optim. Boning, D.S., +, *T-SEM May 94* 233-244

Design centering

chem. amplified resist proc. control, design optim. method. Pan, S., +, *T-SEM Aug 94* 325-332

Detection; cf. Fault diagnosis

Detectors

MMST mfg. technol., hardware, sens., and procs. Barna, G.G., +, *T-SEM May 94* 149-158

rapid thermal multiprocessing for prog. factory in IC mfg. Saraswat, K.C., +, *T-SEM May 94* 159-175

Diagnosis; cf. Fault diagnosis

Dielectric breakdown; cf. Electrostatic discharges

Distributed computing

MMST CIM syst. framework for semicond. wafer fab. McGehee, J., +, *T-SEM May 94* 107-116

E

Electrochemical processes

CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. Parks, H.G., +, *T-SEM Aug 94* 249-258

Electrostatic discharges

static charge removal, isopropyl alcohol soln. Ohmi, T., +, *T-SEM Nov 94* 440-446

EPROM (electrically programmable read-only memory); cf. Read-only memories

ESD; cf. Electrostatic discharges

Etching

CMOSFETs, integrated proc. of MOS gate dielec. structs. Rubloff, G.W., +, *T-SEM Feb 94* 96-100

MMST mfg. technol., hardware, sens., and procs. Barna, G.G., +, *T-SEM May 94* 149-158

MOSFET gate oxide damage, eval. tech., TEM and photon emission. Uraoka, Y., +, *T-SEM Aug 94* 293-297

neural network model develop. for plasma etching proc. Huang, Y.L., +, *T-SEM Aug 94* 333-344

plasma etching, optimal neural network proc. model. Byungwhan Kim, +, *T-SEM Feb 94* 12-21

plasma etch proc., stat. feedback control. Mozumder, P.K., +, *T-SEM Feb 94* 1-11

polysilicon gate etch proc. control in MOS device mfg. Butler, S.W., +, *T-SEM May 94* 193-201

F

Fabrication; cf. Integrated circuit fabrication; Semiconductor device fabrication

Failure analysis

ULSI contamination control, scaling law considerations. Hiraiwa, A., +, *T-SEM Feb 94* 60-67

Fault diagnosis

semicond. mfg. equipt. and procs., diagnosis. Saxena, S., +, *T-SEM May 94* 220-232

Feedback systems

PECVD monitor wafer based controller for semicond. procs. Mozumder, P.K., +, *T-SEM Aug 94* 400-411

RTP semicond. device mfg. equip., real-time multivariable control. Schaper, C., +, *T-SEM May 94* 202-219

FET integrated circuits; cf. CMOS integrated circuits; MOS integrated circuits

FET integrated circuits, memory; cf. CMOS integrated circuits, memory FETs; cf. MOSFETs

Films; cf. Conducting films; Semiconductor films

Flexible manufacturing systems

rapid thermal multiprocessing for prog. factory in IC mfg. Saraswat, K.C., +, *T-SEM May 94* 159-175

RTP semicond. device mfg. equip., real-time multivariable control. Schaper, C., +, *T-SEM May 94* 202-219

Flow control; cf. Fluid flow control

Fluid flow control

mass flow controllers in semicond. mfg., fuzzy logic syst. Ramamurthi, R.K., *T-SEM Feb 94* 42-52

Focusing; cf. Optical-beam focusing

Forecasting

yield, mound defect modeling. de Gyvez, J.P., *T-SEM Nov 94* 430-439

Fourier spectroscopy

situ semicond. materials charactn. emission FT IR spectrosc. Zhen-Hong Zhou, +, *T-SEM Feb 94* 87-91

Furnaces; cf. Process heating

Fuzzy control

mass flow controllers in semicond. mfg., fuzzy logic syst. Ramamurthi, R.K., *T-SEM Feb 94* 42-52

G

Geometrical optics

hexagonal-shaped RTP syst. using vert. tube, develop. Byung Jin Cho, +, *T-SEM Aug 94* 345-353

H

High-speed circuits/devices

graft-base lateral diffusion depth in high-perform. bipolar transistors. Tamaki, Y., +, *T-SEM Aug 94* 279-283

I

IEEE Transactions on Semiconductor Manufacturing; cf. Awards

Infrared spectroscopy

situ semicond. materials charactn. emission FT IR spectrosc. Zhen-Hong Zhou, +, *T-SEM Feb 94* 87-91

Inspection, visual

laser ablation proc. tech. for metallic/polymer layered struct. Guzzo, E.E., +, *T-SEM Feb 94* 73-78

Inspection, visual; cf. Automated optical inspection

Integrated circuit bonding

ball bond inspection/2-D bonding wire profiling, vision system. Khotanzad, A., +, *T-SEM Nov 94* 413-422

fine pitch-long wire assembly, wire bond loop profile develop. Groover, R., +, *T-SEM Aug 94* 393-399

Integrated circuit design

fine pitch-long wire assembly, wire bond loop profile develop. Groover, R., +, *T-SEM Aug 94* 393-399

Integrated circuit fabrication

chem. amplified resist proc. control, design optim. method. Pan, S., +, *T-SEM Aug 94* 325-332

CMOS IC designs, manufacturability modeling, proc. params. Boskin, E.D., +, *T-SEM Aug 94* 298-305

CMOS stat. MOSFET model, IC mfg. proc. fluc., worst case design. Power, J.A., +, *T-SEM Aug 94* 306-318

CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. Parks, H.G., +, *T-SEM Aug 94* 249-258

defect size distrib. in IC layer, test struct. data. Khare, J.B., +, *T-SEM Aug 94* 354-368

hexagonal-shaped RTP syst. using vert. tube, develop. Byung Jin Cho, +, *T-SEM Aug 94* 345-353

MMST IC mfg. equip. control, situ spectral ellipsometry. Maung, S., +, *T-SEM May 94* 184-192

MMST machine control archit. for semicond. mfg. facilities. Beaver, R., +, *T-SEM May 94* 127-133

MMST mfg. technol., hardware, sens., and procs. Barna, G.G., +, *T-SEM May 94* 149-158

PECVD monitor wafer based controller for semicond. procs. Mozumder, P.K., +, *T-SEM Aug 94* 400-411

plasma etching proc., neural network model develop. Huang, Y.L., +, *T-SEM Aug 94* 333-344

- polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W.*, + , *T-SEM May 94* 193-201
- rapid thermal multiprocessing for prog. factory in IC mfg. *Saraswat, K.C.*, + , *T-SEM May 94* 159-175
- real defect outlines and param. extraction, IC checkerboard test struct. *Hess, C.*, + , *T-SEM Aug 94* 284-292
- RTP semicond. device mfg. equip., real-time multivariable control. *Schaper, C.*, + , *T-SEM May 94* 202-219
- run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M.*, + , *T-SEM May 94* 134-148
- SEU/SRAM, CMOS proc. monitor. *Blaes, B.R.*, + , *T-SEM Aug 94* 319-324
- single-wafer cluster tool perform., throughput anal. *Perkinson, T.L.*, + , *T-SEM Aug 94* 369-373
- ULSI contact-hole resist patterns, surface-act. developer, resoln. and lin. *Shimada, H.*, + , *T-SEM Aug 94* 389-393
- Integrated circuit fabrication; cf.** Etching; Integrated circuit bonding; Integrated circuit manufacture; Integrated circuit metallization; Lithography; Masks; Rapid thermal processing; Resists
- Integrated circuit interconnections**
ball bond inspection/2-D bonding wire profiling, vision system. *Khotanzad, A.*, + , *T-SEM Nov 94* 413-422
- Integrated circuit manufacture**
diagnosis of semicond. mfg. equipt. and procs. *Saxena, S.*, + , *T-SEM May 94* 220-232
forecasting yield, mound defect modeling. *de Gyvez, J.P.*, *T-SEM Nov 94* 430-439
LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K.*, + , *T-SEM Feb 94* 53-59
mass flow controllers in semicond. mfg., fuzzy logic syst. *Ramamurthi, R.K.*, *T-SEM Feb 94* 42-52
microelectronics manufacturing science and technology (special issue). *T-SEM May 94* 106-244
MMST CIM syst. framework for semicond. wafer fab. *McGehee, J.*, + , *T-SEM May 94* 107-116
scheduler and planner for semicond. mfg. *Fargher, H.E.*, + , *T-SEM May 94* 117-126
static charge removal, isopropyl alcohol soln. *Ohmi, T.*, + , *T-SEM Nov 94* 440-446
ULSI contamination control, scaling law considerations. *Hiraiwa, A.*, + , *T-SEM Feb 94* 60-67
- Integrated circuit manufacture; cf.** Etching; Integrated circuit fabrication; Lithography; Masks; Rapid thermal processing; Resists
- Integrated circuit measurements**
CMOS IC designs, manufacturability modeling, proc. params. *Boskin, E.D.*, + , *T-SEM Aug 94* 298-305
CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. *Parks, H.G.*, + , *T-SEM Aug 94* 249-258
nanometer-level overlay and feature-placement metrology, test struct. *Cresswell, M.W.*, + , *T-SEM Aug 94* 266-271
real defect outlines and param. extraction, IC checkerboard test struct. *Hess, C.*, + , *T-SEM Aug 94* 284-292
submicron LDD p-MOSFETs, poly-Si gate reentrant detect. *Pan, Y.*, + , *T-SEM Nov 94* 460-462
ULSI contact-hole resist patterns, surface-act. developer, resoln. and lin. *Shimada, H.*, + , *T-SEM Aug 94* 389-393
- Integrated circuit metallization**
CMOS EPROM IC devices, 0.85- μm , conventional contact interconnect technol. *Farahani, M.M.*, + , *T-SEM Feb 94* 79-86
- Integrated circuit metallization; cf.** Integrated circuit interconnections
- Integrated circuit modeling**
CMOS stat. MOSFET model, IC mfg. proc. fluc., worst case design. *Power, J.A.*, + , *T-SEM Aug 94* 306-318
ULSI contamination control, scaling law considerations. *Hiraiwa, A.*, + , *T-SEM Feb 94* 60-67
- Integrated circuit radiation effects**
SEU/SRAM, CMOS proc. monitor. *Blaes, B.R.*, + , *T-SEM Aug 94* 319-324
- Integrated circuit reliability**
static charge removal, isopropyl alcohol soln. *Ohmi, T.*, + , *T-SEM Nov 94* 440-446
ULSI contamination control, scaling law considerations. *Hiraiwa, A.*, + , *T-SEM Feb 94* 60-67
- Integrated circuits; cf.** Large-scale integration; MOS integrated circuits
- Integrated circuit testing**
CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. *Parks, H.G.*, + , *T-SEM Aug 94* 249-258
defect size distrib. in IC layer, test struct. data. *Khare, J.B.*, + , *T-SEM Aug 94* 354-368
ICMTS '93, selected papers (special issue). *T-SEM Aug 94* 246-324
nanometer-level overlay and feature-placement metrology, test struct. *Cresswell, M.W.*, + , *T-SEM Aug 94* 266-271

Intelligent control

- mass flow controllers in semicond. mfg., fuzzy logic syst. *Ramamurthi, R.K.*, *T-SEM Feb 94* 42-52

Interconnections, integrated circuits; cf. Integrated circuit interconnections
Interferometry; cf. Optical interferometry
ISO; cf. Open Systems Interconnection

L

Large-scale integration

- CMOS IC designs, manufacturability modeling, proc. params. *Boskin, E.D.*, + , *T-SEM Aug 94* 298-305

Large-scale integration; cf. Ultra-large-scale integration; Very-large-scale integration

Laser applications, materials processing; cf. Ablation

Learning control systems

- mass flow controllers in semicond. mfg., fuzzy logic syst. *Ramamurthi, R.K.*, *T-SEM Feb 94* 42-52

Learning systems

- plasma etching, optimal neural network proc. model. *Byungwhan Kim*, + , *T-SEM Feb 94* 12-21

Lithography

- MMST mfg. technol., hardware, sens., and procs. *Barna, G.G.*, + , *T-SEM May 94* 149-158
nanometer-level overlay and feature-placement metrology, test struct. *Cresswell, M.W.*, + , *T-SEM Aug 94* 266-271

Lithography; cf. X-ray lithography

LSI; cf. Large-scale integration

M

Machine vision

- IC ball bond inspection/2-D bonding wire profiling, vision system. *Khotanzad, A.*, + , *T-SEM Nov 94* 413-422

Manufacturing automation; cf. Automatic optical inspection; Computer-integrated manufacturing; Flexible manufacturing systems

Manufacturing automation software

- semicond. mfg. plants, efficient scheduling policies, cycle-time mean/variance. *Lu, S.C.H.*, + , *T-SEM Aug 94* 374-388

Manufacturing data processing

- MMST CIM syst. framework for semicond. wafer fab. *McGehee, J.*, + , *T-SEM May 94* 107-116
semicond. mfg., planner and scheduler. *Fargher, H.E.*, + , *T-SEM May 94* 117-126

Manufacturing planning

- semicond. mfg., planner and scheduler. *Fargher, H.E.*, + , *T-SEM May 94* 117-126

Manufacturing scheduling

- MMST CIM syst. framework for semicond. wafer fab. *McGehee, J.*, + , *T-SEM May 94* 107-116
semicond. mfg., planner and scheduler. *Fargher, H.E.*, + , *T-SEM May 94* 117-126
semicond. mfg. plants, efficient scheduling policies, cycle-time mean/variance. *Lu, S.C.H.*, + , *T-SEM Aug 94* 374-388

Manufacturing testing

- defect size distrib. in IC layer, test struct. data. *Khare, J.B.*, + , *T-SEM Aug 94* 354-368
real defect outlines and param. extraction, IC checkerboard test struct. *Hess, C.*, + , *T-SEM Aug 94* 284-292
SEU/SRAM, CMOS proc. monitor. *Blaes, B.R.*, + , *T-SEM Aug 94* 319-324

Masks

- nanometer-level overlay and feature-placement metrology, test struct. *Cresswell, M.W.*, + , *T-SEM Aug 94* 266-271
ULSI contact-hole resist patterns, surface-act. developer, resoln. and lin. *Shimada, H.*, + , *T-SEM Aug 94* 389-393

Mass spectroscopy

- VLSI manufacture, metallic contamination, post-wet-cleaning chem. anal. *Mizokami, Y.*, + , *T-SEM Nov 94* 447-453

Measurement; cf. Integrated circuit measurements; Semiconductor device measurements; Semiconductor materials measurements; Thickness measurement

Mechanical variables control; cf. Fluid flow control

Mechanical variables measurement; cf. Thickness measurement

Memories; cf. Read-only memories; SRAM chips

Memory fault diagnosis

- SEU/SRAM, CMOS proc. monitor. *Blaes, B.R.*, + , *T-SEM Aug 94* 319-324

- Metallization; cf.** Integrated circuit metallization; Semiconductor device metallization
- Microelectronic Test Structures, 1993 IEEE Int. Conf. on**
selected papers (special issue). *T-SEM Aug 94* 246-324
- Minimization methods; cf.** Optimization methods
- MISFETs; cf.** MOSFETs
- Modeling**
forecasting yield, mound defect modeling. *de Gyvez, J.P., T-SEM Nov 94* 430-439
single-wafer cluster tool perform., throughput anal. *Perkinson, T.L., +, T-SEM Aug 94* 369-373
- Modeling; cf.** Circuit simulation; Integrated circuit modeling; Semiconductor device modeling; Semiconductor process modeling
- Monitoring; cf.** Process monitoring
- Monte Carlo methods**
LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K., +, T-SEM Feb 94* 53-59
- MOSFET circuits; cf.** MOS integrated circuits
- MOSFETs**
deep sub-micron MOSFETs, dyn. design proc. for yield enhancement. *Sitte, R., +, T-SEM Feb 94* 92-96
gate oxide damage, plasma proc., TEM, photon emission. *Uraoka, Y., +, T-SEM Aug 94* 293-297
LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K., +, T-SEM Feb 94* 53-59
LOCOS/-trench-isolated MOSFETs, channel-width meas. by photoemission. *Ohzone, T., +, T-SEM Aug 94* 259-265
submicron LDD p-MOSFETs, poly-Si gate reentrant detect. *Pan, Y., +, T-SEM Nov 94* 460-462
- MOSFETs; cf.** CMOSFETs
- MOS integrated circuits**
LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K., +, T-SEM Feb 94* 53-59
polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W., +, T-SEM May 94* 193-201
- MOS integrated circuits; cf.** CMOS integrated circuits
- MOS integrated circuits, memory; cf.** CMOS integrated circuits, memory
- Multivariable systems**
PECVD monitor wafer based controller for semicond. procs. *Mozumder, P.K., +, T-SEM Aug 94* 400-411
RTP semicond. device mfg. equip., real-time multivariable control. *Schaper, C., +, T-SEM May 94* 202-219

N

- Neural network applications**
plasma etching, optimal neural network proc. model. *Byungwhan Kim, +, T-SEM Feb 94* 12-21
plasma etching proc., neural network model develop. *Huang, Y.L., +, T-SEM Aug 94* 333-344
- Numerical methods; cf.** Monte Carlo methods; Optimization methods

O

- Object-oriented methods**
run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M., +, T-SEM May 94* 134-148
- Open Systems Interconnection**
MMST CIM syst. framework for semicond. wafer fab. *McGehee, J., +, T-SEM May 94* 107-116
- Optical-beam focusing**
Gaudi test struct., determine optimum focus. *Fallon, M., +, T-SEM Aug 94* 272-278
- Optical interferometry**
nanometer-level overlay and feature-placement metrology, test struct. *Cresswell, M.W., +, T-SEM Aug 94* 266-271
- Optical transducers**
MMST IC mfg. equip. control, situ spectral ellipsometry. *Maung, S., +, T-SEM May 94* 184-192
- Optimization methods**
chem. amplified resist proc. control, design optim. method. *Pan, S., +, T-SEM Aug 94* 325-332
DOE/Opt syst. for semicond. mfg. proc./device modelling/optim. *Boning, D.S., +, T-SEM May 94* 233-244
IC proc. optim., simul./response surface methodology integrat. *Gaston, G.J., +, T-SEM Feb 94* 22-33
RTP lamp design, optim. *Cho, Y.M., +, T-SEM Feb 94* 34-41

OSI; cf. Open Systems Interconnection

P

- Packaging; cf.** Plastic packaging
- Particle spectroscopy; cf.** Mass spectroscopy
- Plastic packaging**
fine pitch-long wire assembly, wire bond loop profile develop. *Groover, R., +, T-SEM Aug 94* 393-399
- Prediction methods; cf.** Forecasting
- Predictive control**
polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W., +, T-SEM May 94* 193-201
- Process control**
chem. amplified resist proc. control, design optim. method. *Pan, S., +, T-SEM Aug 94* 325-332
plasma etch proc., stat. feedback control. *Mozumder, P.K., +, T-SEM Feb 94* 1-11
polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W., +, T-SEM May 94* 193-201
run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M., +, T-SEM May 94* 134-148
- Process control; cf.** Process monitoring
- Process heating**
semicond. wafer temp. distrib., hot-wall rapid diffusion furnace heating. *Hirasawa, S., +, T-SEM Nov 94* 423-429
- Process monitoring**
CMOS IC designs, manufacturability modeling, proc. params. *Boskin, E.D., +, T-SEM Aug 94* 298-305
MMST IC mfg. equip. control, situ spectral ellipsometry. *Maung, S., +, T-SEM May 94* 184-192
MMST mfg. technol., hardware, sens., and procs. *Barna, G.G., +, T-SEM May 94* 149-158
PECVD monitor wafer based controller for semicond. procs. *Mozumder, P.K., +, T-SEM Aug 94* 400-411
rapid thermal multiprocessing for prog. factory in IC mfg. *Saraswat, K.C., +, T-SEM May 94* 159-175
semicond. mfg. plants, efficient scheduling policies, cycle-time mean/variance. *Lu, S.C.H., +, T-SEM Aug 94* 374-388
SEU/DRAM, CMOS proc. monitor. *Blaes, B.R., +, T-SEM Aug 94* 319-324

Q

- Quality control**
plasma etch proc., stat. feedback control. *Mozumder, P.K., +, T-SEM Feb 94* 1-11
- Quartz materials/devices**
hexagonal-shaped RTP syst. using vert. tube, develop. *Byung Jin Cho, +, T-SEM Aug 94* 345-353

R

- Radiation effects; cf.** Integrated circuit radiation effects
- Rapid thermal processing**
CVD simul., model-based temp. control. *Sorrell, F.Y., +, T-SEM Nov 94* 454-459
hexagonal-shaped RTP syst. using vert. tube, develop. *Byung Jin Cho, +, T-SEM Aug 94* 345-353
lamp design optim. in RTP. *Cho, Y.M., +, T-SEM Feb 94* 34-41
multiprocessing for prog. factory in IC mfg. *Saraswat, K.C., +, T-SEM May 94* 159-175
semicond. device mfg., RTP real-time control strategy. *Schaper, C., +, T-SEM May 94* 202-219
semicond. wafer temp. distrib., hot-wall rapid diffusion furnace heating. *Hirasawa, S., +, T-SEM Nov 94* 423-429
temp. uniformity, 3D effects. *Knutson, K.L., +, T-SEM Feb 94* 68-72
- Random-access memories; cf.** SRAM chips
- Ray optics; cf.** Geometrical optics
- Read-only memories**
CMOS EPROM IC devices, 0.85- μm , conventional contact interconnect technol. *Farahani, M.M., +, T-SEM Feb 94* 79-86
- Real-time systems**
MMST IC mfg. equip. control, situ spectral ellipsometry. *Maung, S., +, T-SEM May 94* 184-192
rapid thermal multiprocessing for prog. factory in IC mfg. *Saraswat, K.C., +, T-SEM May 94* 159-175
RTP semicond. device mfg. equip., real-time multivariable control. *Schaper, C., +, T-SEM May 94* 202-219

semicond. mfg., planner and scheduler. *Fargher, H.E.*, +, *T-SEM May 94* 117-126

Reliability; cf. Failure analysis; Semiconductor device reliability

Resistance; cf. Contact resistance

Resists

chem. amplified resist proc. control, design optim. method. *Pan, S.*, +, *T-SEM Aug 94* 325-332

ULSI contact-hole resist patterns, surface-act. developer, resoln. and lin. *Shimada, H.*, +, *T-SEM Aug 94* 389-393

ROM; cf. Read-only memories

S

Scheduling; cf. Manufacturing scheduling

Semiconductor device bonding; cf. Integrated circuit bonding

Semiconductor device breakdown

LOCOS/-trench-isolated MOSFETs, channel-width meas. by photoemission. *Ohzone, T.*, +, *T-SEM Aug 94* 259-265

MOSFET gate oxide damage, eval. tech., TEM and photon emission. *Uraoka, Y.*, +, *T-SEM Aug 94* 293-297

Semiconductor device fabrication

CMOSFETs, integrated proc. of MOS gate dielec. structs. *Rubloff, G.W.*, +, *T-SEM Feb 94* 96-100

deep sub-micron MOSFETs, dyn. design proc. for yield enhancement. *Sitte, R.*, +, *T-SEM Feb 94* 92-96

Gaudi test struct., determine optimum focus. *Fallon, M.*, +, *T-SEM Aug 94* 272-278

laser ablation proc. tech. for metallic/polymer layered struct. *Guzzo, E.E.*, +, *T-SEM Feb 94* 73-78

MMST machine control archit. for semicond. mfg. facilities. *Beaver, R.*, +, *T-SEM May 94* 127-133

MOSFET gate oxide damage, eval. tech., TEM and photon emission. *Uraoka, Y.*, +, *T-SEM Aug 94* 293-297

plasma etching, optimal neural network proc. model. *Byungwhan Kim*, +, *T-SEM Feb 94* 12-21

plasma etch proc., stat. feedback control. *Mozumder, P.K.*, +, *T-SEM Feb 94* 1-11

RTP of 8-inch wafers, 3D effects on temp. uniformity. *Knutson, K.L.*, +, *T-SEM Feb 94* 68-72

RTP semicond. device mfg. equip., real-time multivariable control. *Schaper, C.*, +, *T-SEM May 94* 202-219

run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M.*, +, *T-SEM May 94* 134-148

semicond. mfg. plants, efficient scheduling policies, cycle-time mean/variance. *Lu, S.C.H.*, +, *T-SEM Aug 94* 374-388

Semiconductor device fabrication; cf. Integrated circuit fabrication; Semiconductor device manufacture

Semiconductor device manufacture

diagnosis of semicond. mfg. equipt. and procs. *Saxena, S.*, +, *T-SEM May 94* 220-232

LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K.*, +, *T-SEM Feb 94* 53-59

mass flow controllers in semicond. mfg., fuzzy logic syst. *Ramamurthi, R.K.*, *T-SEM Feb 94* 42-52

microelectronics manufacturing science and technology (special issue). *T-SEM May 94* 106-244

MMST CIM syst. framework for semicond. wafer fab. *McGehee, J.*, +, *T-SEM May 94* 107-116

scheduler and planner for semicond. mfg. *Fargher, H.E.*, +, *T-SEM May 94* 117-126

wafer temp. distrib., hot-wall rapid diffusion furnace heating. *Hirasawa, S.*, +, *T-SEM Nov 94* 423-429

Semiconductor device manufacture; cf. Integrated circuit manufacture; Semiconductor device fabrication

Semiconductor device measurements

graft-base lateral diffusion depth in high-perform. bipolar transistors. *Tamaki, Y.*, +, *T-SEM Aug 94* 279-283

LOCOS/-trench-isolated MOSFETs, channel-width meas. by photoemission. *Ohzone, T.*, +, *T-SEM Aug 94* 259-265

MOSFET gate oxide damage, eval. tech., TEM and photon emission. *Uraoka, Y.*, +, *T-SEM Aug 94* 293-297

Semiconductor device measurements; cf. Integrated circuit measurements

Semiconductor device metallization; cf. Integrated circuit metallization

Semiconductor device modeling

CMOS stat. MOSFET model, IC mfg. proc. fluctuations, worst case design. *Power, J.A.*, +, *T-SEM Aug 94* 306-318

DOE/Opt syst. for semicond. mfg. proc./device modelling/optim. *Boning, D.S.*, +, *T-SEM May 94* 233-244

submicron LDD p-MOSFETs, poly-Si gate reentrant detect. *Pan, Y.*, +, *T-SEM Nov 94* 460-462

Semiconductor device modeling; cf. Integrated circuit modeling

Semiconductor device radiation effects; cf. Integrated circuit radiation effects

Semiconductor device reliability; cf. Integrated circuit reliability

Semiconductor device testing

graft-base lateral diffusion depth in high-perform. bipolar transistors. *Tamaki, Y.*, +, *T-SEM Aug 94* 279-283

ICMTS '93, selected papers (special issue). *T-SEM Aug 94* 246-324

LOCOS/-trench-isolated MOSFETs, channel-width meas. by photoemission. *Ohzone, T.*, +, *T-SEM Aug 94* 259-265

MOSFET gate oxide damage, eval. tech., TEM and photon emission. *Uraoka, Y.*, +, *T-SEM Aug 94* 293-297

Semiconductor device testing; cf. Integrated circuit testing

Semiconductor device thermal factors

wafer temp. distrib., hot-wall rapid diffusion furnace heating. *Hirasawa, S.*, +, *T-SEM Nov 94* 423-429

Semiconductor device thermal factors; cf. Rapid thermal processing

Semiconductor films

situ semicond. materials charactn. emission FT IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Feb 94* 87-91

Semiconductor growth

RTP, CVD simul., model-based temp. control. *Sorrell, F.Y.*, +, *T-SEM Nov 94* 454-459

situ semicond. materials charactn. emission FT IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Feb 94* 87-91

Semiconductor materials measurements

situ semicond. materials charactn. emission FT IR spectrosc. *Zhen-Hong Zhou*, +, *T-SEM Feb 94* 87-91

Semiconductor process modeling

CMOS IC designs, manufacturability modeling, proc. params. *Boskin, E.D.*, +, *T-SEM Aug 94* 298-305

CMOS stat. MOSFET model, IC mfg. proc. fluctuations, worst case design. *Power, J.A.*, +, *T-SEM Aug 94* 306-318

CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. *Parks, H.G.*, +, *T-SEM Aug 94* 249-258

deep sub-micron MOSFETs, dyn. design proc. for yield enhancement. *Sitte, R.*, +, *T-SEM Feb 94* 92-96

diagnosis of semicond. mfg. equipt. and procs. *Saxena, S.*, +, *T-SEM May 94* 220-232

DOE/Opt syst. for semicond. mfg. proc./device modelling/optim. *Boning, D.S.*, +, *T-SEM May 94* 233-244

IC proc. optim., simul./response surface methodology integrat. *Gaston, G.J.*, +, *T-SEM Feb 94* 22-33

plasma etching, optimal neural network proc. model. *Byungwhan Kim*, +, *T-SEM Feb 94* 12-21

polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W.*, +, *T-SEM May 94* 193-201

RTP, CVD simul., model-based temp. control. *Sorrell, F.Y.*, +, *T-SEM Nov 94* 454-459

RTP lamp design, optim. *Cho, Y.M.*, +, *T-SEM Feb 94* 34-41

RTP of 8-inch wafers, 3D effects on temp. uniformity. *Knutson, K.L.*, +, *T-SEM Feb 94* 68-72

run-to-run supervisory proc. control syst. archit., semicond. mfg. appl. *Sullivan, M.*, +, *T-SEM May 94* 134-148

SiN_x, computational fluid dyn. model for PECVD. *Collins, D.J.*, +, *T-SEM May 94* 176-183

Sensitivity

IC proc. optim., simul./response surface methodology integrat. *Gaston, G.J.*, +, *T-SEM Feb 94* 22-33

LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K.*, +, *T-SEM Feb 94* 53-59

Silicon materials/devices

plasma etching proc., neural network model develop. *Huang, Y.L.*, +, *T-SEM Aug 94* 333-344

polysilicon gate etch proc. control in MOS device mfg. *Butler, S.W.*, +, *T-SEM May 94* 193-201

SiN_x, computational fluid dyn. model for PECVD. *Collins, D.J.*, +, *T-SEM May 94* 176-183

Simulation

hexagonal-shaped RTP syst. using vert. tube, develop. *Byung Jin Cho*, +, *T-SEM Aug 94* 345-353

Simulation

Simulation; cf. Circuit simulation

Size measurement; cf. Thickness measurement

Software; cf. Manufacturing automation software

Special issues/sections

ICMTS '93, selected papers. *T-SEM Aug 94* 246-324

microelectronics manufacturing science and technology. *T-SEM May 94* 106-244

Spectroscopy; cf. Fourier spectroscopy; Infrared spectroscopy; Mass spectroscopy; X-ray spectroscopy

SRAM chips

SEU/SRAM, CMOS proc. monitor. *Blaes, B.R., + , T-SEM Aug 94 319-324*

Statistics

CMOS stat. MOSFET model, IC mfg. proc. flucst., worst case design. *Power, J.A., + , T-SEM Aug 94 306-318*

defect size distribst. in IC layer, test struct. data. *Khare, J.B., + , T-SEM Aug 94 354-368*

LDD MOSFETs, 0.35 μm devices, mfg. sensitivity anal. *Hasnat, K., + , T-SEM Feb 94 53-59*

SEU/SRAM, CMOS proc. monitor. *Blaes, B.R., + , T-SEM Aug 94 319-324*

T

Temperature calculations

hexagonal-shaped RTP syst. using vert. tube, develop. *Byung Jin Cho, + , T-SEM Aug 94 345-353*

RTP of 8-inch wafers, 3D effects on temp. uniformity. *Knutson, K.L., + , T-SEM Feb 94 68-72*

Temperature control

RTP, CVD simul., model-based temp. control. *Sorrell, F.Y., + , T-SEM Nov 94 454-459*

RTP semicond. device mfg. equip., real-time multivariable control. *Schaper, C., + , T-SEM May 94 202-219*

Temperature control; cf.

 Process heating

Testing; cf. Integrated circuit testing; Manufacturing testing; Semiconductor device testing

Thermal factors

hexagonal-shaped RTP syst. using vert. tube, develop. *Byung Jin Cho, + , T-SEM Aug 94 345-353*

Thermal factors; cf. Ablation; Rapid thermal processing; Semiconductor device thermal factors; Temperature calculations; Temperature control

Thickness measurement

situ semicond. materials charactn. emission FT IR spectrosc. *Zhen-Hong Zhou, + , T-SEM Feb 94 87-91*

Transducers; cf.

 Optical transducers

Transient analysis

single-wafer cluster tool perform., throughput anal. *Perkinson, T.L., + , T-SEM Aug 94 369-373*

Transistors; cf.

 Bipolar transistors

U

Ultra-large-scale integration

CMOS ULSI homog. metal contamination, test struct. metrology and device modeling. *Parks, H.G., + , T-SEM Aug 94 249-258*

metallic contamination, post-wet-cleaning chem. anal. *Mizokami, Y., + , T-SEM Nov 94 447-453*

ULSI contact-hole resist patterns, surface-act. developer, resoln. and lin. *Shimada, H., + , T-SEM Aug 94 389-393*

ULSI contamination control, scaling law considerations. *Hiraiwa, A., + , T-SEM Feb 94 60-67*

V

Very-large-scale integration

CMOS EPROM IC devices, 0.85- μm , conventional contact interconnect technol. *Farahani, M.M., + , T-SEM Feb 94 79-86*

fine pitch-long wire assembly, wire bond loop profile develop. *Groover, R., + , T-SEM Aug 94 393-399*

Vision systems (nonbiological); cf. Inspection, visual; Machine vision

W

Wiring; cf. Integrated circuit interconnections

X

X-ray lithography

chem. amplified resist proc. control, design optim. method. *Pan, S., + , T-SEM Aug 94 325-332*

X-ray spectroscopy

VLSI manufacture, metallic contamination, post-wet-cleaning chem. anal. *Mizokami, Y., + , T-SEM Nov 94 447-453*

Y

Yield optimization

deep sub-micron MOSFETs, dyn. design proc. for yield enhancement. *Sitte, R., + , T-SEM Feb 94 92-96*

fine pitch-long wire assembly, wire bond loop profile develop. *Groover, R., + , T-SEM Aug 94 393-399*

forecasting yield, mound defect modeling. *de Gyvez, J.P., T-SEM Nov 94 430-439*

real defect outlines and param. extraction, IC checkerboard test struct. *Hess, C., + , T-SEM Aug 94 284-292*

INFORMATION FOR AUTHORS

Content

The IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING is published quarterly with the first issue in February. Contributed papers may be of a tutorial or research nature, but the latter must be original and must not duplicate descriptions or derivations available elsewhere.

This TRANSACTIONS aims to address the challenging problems of manufacturing complex microelectronic components, especially very large scale integrated circuits (VLSI), but also thin-film heads for magnetic recording, integrated optical components, and other similar products. Manufacturing these products typically requires precision micropatterning, precision control of materials properties, ultra-clean work environments, and complex interactions of chemical, physical, electrical, and mechanical processes. An integrated application of interdisciplinary skills is essential for success.

Particularly sought for these TRANSACTIONS are original papers describing practical engineering techniques for solving problems involving interactions among facility, equipment, process, product, and people issues in the context of manufacturing. The TRANSACTIONS' spectrum of coverage will range from fundamental to applied. Whenever possible papers should include appropriate results from manufacturing experience. Submission of a manuscript manifests the fact that it has been neither copyrighted, published, nor submitted or accepted for publication elsewhere, unless otherwise so stated by the author.

Length

Authors should document their work in relation to the open literature. The following limits on length will be enforced.

- 1) Regular papers, 7 to 20 double-spaced pages in length, plus up to 10 pages, 8.5" by 11" of figures.
- 2) Correspondence items of less than 6 double-spaced pages, plus not more than 3 pages of figures.

Style for Manuscripts

- 1) The manuscript should be printed using double space; use one side of the sheet only. Office-duplicated copies are acceptable.
- 2) Provide a carefully worded abstract of from 100 to 200 words for papers and less than 50 words for correspondence. Name, address, and telephone number of author(s) should appear with abstract.
- 3) A pamphlet, "Information for IEEE Transactions and Journal Authors," is available on request from the IEEE Operations Center, 445 Hoes Lane, P.O. Box 1331, Piscataway, NJ 08855-1331.
- 4) References may appear as numbered footnotes or in a separate bibliography at the end of the paper. In either case, references should be complete and in IEEE style.

Style for papers: Author (with initials first), title, journal title, volume number, inclusive page numbers, month, year.

Style for books: Author, title, location, publisher, year, page or chapter number (if desired). See this issue for further examples.

- 5) Figure captions should be on a separate sheet in proper style for typesetting. See this issue for examples.
- 6) Departures from the above style may delay publication.

Style for Illustrations

- 1) Originals of drawings and glossy print photographs should be sharp and of good contrast. Line drawings should be in high contrast black ink on a white background. Use 8.5" by 11" size sheets to simplify handling of the manuscript. Template lettering is recommended; typing on figures is not acceptable. Lettering must be large enough to permit legible reduction of the figure to column width, perhaps as much as 4:1.
- 2) Identify each illustration on the back or at the bottom of the front with the figure number and name of author(s). Captions lettered on figures will be blocked out in reproduction in favor of typeset captions.

Review Process

The review process usually requires about two months. The author is then notified of the decision of the Editor or Associate Editor based on reviewer recommendations. The authors may be asked to modify the manuscript if it is not accepted or rejected in its original form. The elapsed time between final acceptance of a manuscript and publication is usually four to eight months.

Submissions

Send the original and three copies of your manuscript to the Editor. Each copy should be complete with illustrations and should be accompanied by a separate sheet containing the address to which galley proofs and other correspondence can be sent. Also enclose original illustrations or be prepared to submit these immediately upon acceptance of your manuscript. Authors will be charged for changes in text or figures in proof. In the case of regular papers, also be prepared to provide a brief technical biography and photograph of each author.

Electronic Publishing: This form of manuscript handling is available as an option for the accepted letter. At the time of initial submission, the author is requested to submit only the hard copies. Upon final acceptance of the manuscript, the author is encouraged to submit the final version of his manuscript in electronic form on a floppy disk prepared with an acceptable word processor together with an identical paper copy. Figures, photos, etc., must be submitted in a camera ready form but not in an electronic form.

Page Charges: After manuscript has been accepted for publication, the author's company or institution will be requested to pay a charge of \$110.00 per printed page to cover part of the cost of publication. Page charges for this IEEE TRANSACTIONS, like those for journals of other professional societies, are not obligatory nor is their payment a prerequisite for publication. The author will receive 100 free reprints without covers if the charge is honored. Detailed instructions will accompany the galley proof.

Copyright: It is the policy of the IEEE to own the copyright to the technical contributions it publishes on behalf of the interests of the IEEE, its authors, and their employers, and to facilitate the appropriate reuse of this material by others. To comply with the U.S. Copyright Law, authors are required to sign an IEEE copyright transfer form before publication. This form, a copy of which appears in the February 1994 issue of this TRANSACTIONS, returns to authors and their employers full rights to reuse their material for their own purposes. Authors must submit a signed copy of this form with their manuscripts.

